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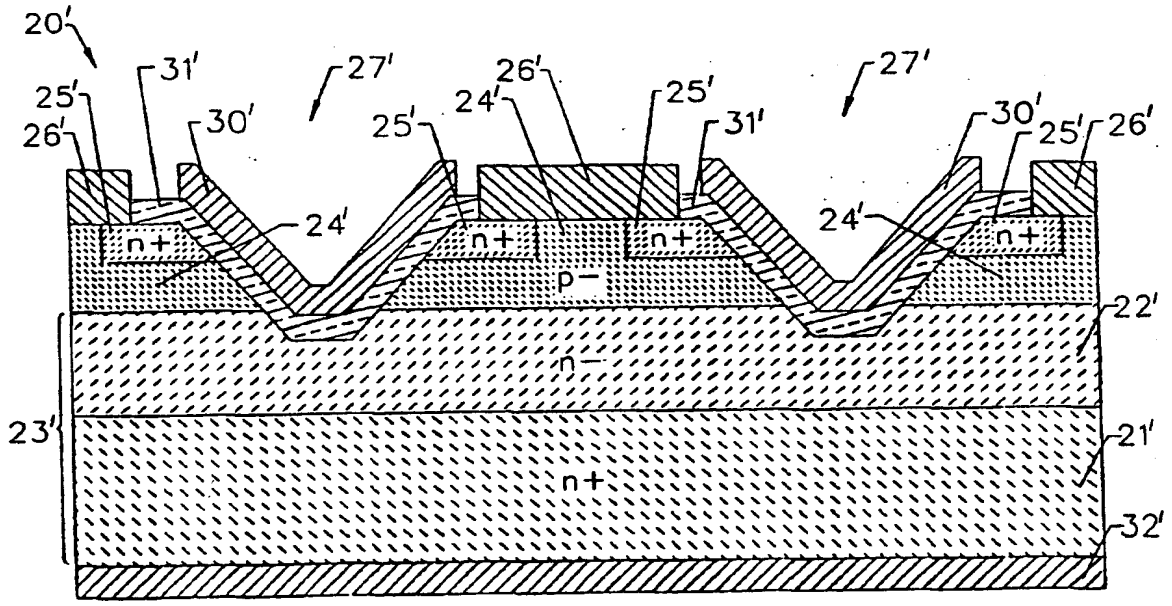


(57) Abstract

The power metal oxide semiconductor field effect transistor (MOSFET) has a drain region, a channel region, and a source region formed of silicon carbide. The drain region has a substrate of silicon carbide of a first conductivity type and a drain-drift region of silicon carbide adjacent the substrate having the same conductivity type. The channel region is adjacent the drain-drift region and has the opposite conductivity type from the drain-drift region. The source region is adjacent the channel region and has the same conductivity type as the drain-drift region. The MOSFET has a gate region having a gate electrode formed on a first portion of the source region, a first portion of the channel region, and a first portion of the drain region. A source electrode is formed on a second portion of the source region and a second portion of the channel region. Also, a drain electrode is formed on a second portion of the drain region.

# POWER MOSFET IN SILICON CARBIDE

## Related Applications

This invention is related to copending U.S. Patent Application Serial No. 07/893,642 filed on June 5, 1992.

## Field Of The Invention

This invention was made at least partially with government support under the National Aeronautical and Space Administration ("NASA"), Contract Number NAS-25956. The government may have certain rights in this invention. This invention relates to power metal oxide semiconductor field effect transistors ("MOSFETs"), and more particularly to a MOSFET formed in silicon carbide.

## Background Of The Invention

Power semiconductor devices, such as high-power bipolar junction transistors ("HPBT"), power metal oxide semiconductor field effect transistors ("MOSFET"), or gate turn-off thyristors ("GTO"), are semiconductor devices that are capable of controlling or passing large amounts of current and blocking high voltages. Power MOSFETS are generally known and one of the most critical parameters for a power MOSFET is the specific on-resistance (i.e., the resistance of the device in the linear region when the device is turned on). The specific on-resistance for a power MOSFET preferably should be as small as possible so as to maximize the source to drain current per unit area for

a given source to drain voltage applied to the MOSFET. The lower the specific on-resistance, the lower the voltage drop is for a given current rating.

Conventional power MOSFETs are manufactured in silicon (Si). MOSFETs formed in Si, however, have certain performance limitations inherent in the Si material itself, such as the thickness of the drain-drift region. The largest contributory factor to specific on-resistance is the resistance of the drain-drift region of the MOSFET. The thickness and doping of the drain-drift region limit the on-resistance. As the rated voltage of a MOSFET is increased, typically the drain-drift region thickness is increased and the drain-drift region doping is decreased. Therefore, the resistance of the drain-drift region increases dramatically. Hence, the thickness of the drain-drift region should be minimized for any given rated voltage so as to minimize the specific on-resistance for the device.

These problems with on-resistance have been recognized and several MOSFET structures have been developed in an attempt to solve the on-resistance problems. Examples of such developments may be seen in U.S. Patent 4,952,991 by Kayuma entitled "*Vertical Field-Effect Transistor Having A High Breakdown Voltage And A Small On-Resistance*"; U.S. Patent 4,959,699 by Lidow, et al. entitled "*High Power MOSFET With Low On-Resistance And High Breakdown Voltage*"; U.S. Patent 4,608,584 by Mihara entitled "*Vertical Type MOS Transistor*"; U.S. Patent 4,931,408 by Hshich entitled "*Method of Fabricating a Short-Channel Low Voltage DMOS Transistor*"; U.S. Patent 4,974059 by Kinzer entitled "*Semiconductor High-Power MOSFET Device*"; U.S. Patent 4,642,666 by Lidow et al. entitled "*High Power MOSFET With Low On-Resistance And High Breakdown Voltage*"; U.S. Patent 4,965,647 by Takahashi entitled "*Vertical MOS Field Effect Transistor Having A High Withstand*

*Voltage And A High Switching Speed*"; U.S. Patent 4,860,084 by Shibata entitled "*Semiconductor Device MOSFET With V-Shaped Drain Contact*"; and U.S. Patent 4,697,201 by Mihara entitled "*Power MOSFET with Decreased Resistance In The Conducting State*". These prior attempts to solve the problem included various structures of the Si semiconductor material to try to lower the on-resistance. These prior attempts, however, failed to adequately understand the inherent limitations in the Si semiconductor material itself.

Thus, to the best of the inventor's knowledge, there presently exists no power MOSFET having low on-resistance and a high temperature range for high voltages.

## Summary Of The Invention

The present invention therefore provides a power MOSFET having a low on-resistance and a high temperature range for high voltages. By understanding and developing material processing techniques in silicon carbide, a power MOSFET formed in silicon carbide provides improvement in on-resistance and high temperature performance over conventional power MOSFETs formed in Si.

More particularly, the power metal oxide semiconductor field effect transistor (MOSFET) has a drain region, a channel region, and a source region formed of silicon carbide. The drain region has a substrate of silicon carbide of a first conductivity type and a drain-drift region of silicon carbide adjacent the substrate having the same conductivity type. The channel region is adjacent the drain-drift region and has the opposite conductivity type from the drain-drift region. The source region is adjacent the channel region and has the same conductivity type as the drain-drift region. The MOSFET also has a gate region having a gate electrode formed adjacent a first portion of the source region, a first portion of the

channel region, and a first portion of the drain region. A source electrode is formed adjacent a second portion of the source region and a second portion of the channel region. A drain electrode is formed on a second portion of the drain region.

## Description Of The Drawings

Some of the features and advantages of the present invention having been stated, others will become apparent as the description proceeds when taken in conjunction with the accompanying drawings, in which:

Figure 1 is a schematic partial cross-sectional view of a vertical MOSFET formed in silicon carbide having a U-shaped gate contact region according to the present invention;

Figure 2 is a schematic partial cross-sectional view of a vertical MOSFET having a v-shaped gate contact region ("VMOSFET") formed in silicon carbide according to another embodiment of the present invention;

Figure 3 is a schematic partial cross-sectional view of a VMOSFET formed in silicon carbide according to a further embodiment of the present invention;

Figure 4 is a schematic partial cross-sectional view of a VMOSFET formed in silicon carbide according to yet another embodiment of the present invention;

Figure 5 is a plot of the drain current-voltage characteristics of a VMOSFET formed in silicon carbide having an active area of $6.7 \times 10^{-4}$ $cm^2$ at a temperature of 300° K;

Figure 6 is a plot of the transconductance - gate voltage characteristics of a VMOSFET according to the present invention;

Figure 7 is a schematic partial cross-sectional view of an ungrounded VMOSFET formed in

silicon carbide according to yet another embodiment of the present invention;

Figure 8 is a plot of the drain current-voltage characteristics of an ungrounded VMOSFET according to the embodiment of Figure 7; and

Figure 9 is a photographic view of the mask used to form the MOSFET according to the present invention.

## Detailed Description

The present invention now will be described more fully hereinafter with reference to the accompanying drawings in which a preferred embodiment of the invention is shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiment set forth herein; rather, this embodiment is provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring now to the drawings, the power MOSFET devices according to the present invention can be fabricated utilizing grounded structures as shown in Figures 1-3. Figure 1 illustrates a schematic cross-sectional view of a power metal oxide semiconductor field effect transistor (MOSFET) formed in silicon carbide having a U-shaped gate contact region broadly designated at **27** according to the present invention. The MOSFET, broadly designated at **20**, has a drain region **23** having a substrate **21** formed of silicon carbide (SiC) of a first conductivity type, which in the illustrated embodiment is shown as n+. The SiC as described herein typically has a 6H polytype, but as will be apparent to those skilled in the art the SiC may consist of other polytypes, including but not limited to the 3C, 2H, 4H or 15R polytypes. The drain region **23** also has a drain-drift region **22** of SiC

having the same conductivity type shown, which in the illustrated embodiment is shown as n-. The n+ and n- regions, as well as p+ and p-, are designated "+" and "-" for heavy and low doping levels respectively of the same material. A channel region **24** is adjacent the drain-drift region **22** of the drain region **23** and has the opposite conductivity type shown as p-. A source region **25** having a source electrode shown as source contact **26** formed adjacent a portion thereof is adjacent the channel region **24** and has the same conductivity type as the drain-drift region **22**, shown as n+. A gate region **27** has a gate electrode shown as gate contact **30** formed adjacent portions of the source region **25**, the channel region **24**, and the drain region **23**. The gate region **27** is formed by trenching into these portions of the source **25**, channel **24**, and drain **23** regions as illustrated. A drain electrode shown as drain contact **32** is also formed adjacent a portion of the drain region **23**.

Also, an insulating layer **31** is formed between the gate contact **30** and the various portions of the source region **25**, the channel region **24**, and the drain region **23**. The insulating layer **31** is typically an oxide layer such as silicon dioxide ($SiO_2$). Further, the MOSFET according to the invention has mesa edge terminations illustrated in Figure 1 along one side thereof and designated at **35**. The mesa edge termination also occurs, but is not shown, in the embodiments illustrated in Figures 2-4 and 7. The mesa edge termination is typically passivated with $SiO_2$, designated at **36**, and may be thicker than other portions of the MOSFET.

Although both carbon-face (C-face) and silicon-face (Si-face) wafers may be fabricated, the C-face wafers are preferred and, hence, are described in detail below. The C-face is more optimal for this device since the oxide layer **31** grown on the top of the

wafer, where the gate contact **30** overlaps the implanted source material and the bottom of the trench, is generally thicker than the oxide layer on the sidewalls because of anisotropic oxidation rates. This provides a thicker oxide where the dielectric failure is most likely, yet allows the oxide on the sidewall to remain relatively thin, which results in better transport properties.

The C-face substrates ($n = 1\text{-}4 \times 10^{18}$ per cubic centimeter ($cm^{-3}$) (1-4E18)) may have epitaxial structures grown in the following manner. The first epilayer grown (not illustrated in the drawings) is a 0.5 micrometer ($\mu m$) thick n+ layer on the substrate **21** for the punch-through of the drain-drift region **22**. The n- drain-drift region **22** is then grown with a doping density ranging from $5\text{-}7 \times 10^{15}$ $cm^{-3}$ (5-7E15) and a thickness of 4.3 $\mu m$. These conditions are designed to sustain a voltage (V) of about 50 V or more of drain bias before punch-through to the n+ layer **21**. The channel layers **24** are grown with carrier concentrations ranging from $7\text{-}15 \times 10^{15}$ $cm^{-3}$ (7-15E15) and a thickness of 2.0 $\mu m$. After the n+ ion implant for the source region **25**, the channel length should be about 1.5 $\mu m$, which should also be able to support 50 V without punch-through to the source region **25**.

The device of Figure 1 is fabricated as follows. First, the outer mesa pattern is reactive ion etched 0.5 $\mu m$ into the SiC surface to act as an alignment mark for future levels. Polysilicon, 0.75 $\mu m$ thick, is then deposited on the wafer, and patterned using reactive ion etching in dichlorodifluoromethane ($CCl_2F_2$). The remaining implant mask is patterned such that an entire wafer is implanted except an undersized pattern of the source contact **26**. The mask is 2.5 $\mu m$ undersized, meaning that the center 10 $\mu m$ of the 15 $\mu m$ wide source contact will be on non-implanted p-type material. The ion implantation of the source wells **25**

is performed by triple implanting $n^+$ at 650 degrees Centigrade (°C) under the following conditions, which results in a 2 x $10^{20}$ $cm^{-3}$ (2E20) peak concentration:

$$E = 40 \text{ keV}, \phi = 1.34 \times 10^{15} \text{ cm}^{-2}$$

$$E = 80 \text{ keV}, \phi = 2.18 \times 10^{15} \text{ cm}^{-2}$$

$$E = 150 \text{ keV}, \phi = 3.10 \times 10^{15} \text{ cm}^{-2}$$

where E is the energy, keV is kilo-electron-volts, and $\phi$ is the dose in atoms/$cm^2$.

After implantation, the polysilicon is stripped and the wafers are annealed at 1500°C in Argon (Ar) for 10 minutes. An Aluminum (Al) layer is then deposited and patterned to open windows for the reactive ion etching of the trenches. This pattern only opens the eight fingers that were 5 $\mu$m x 250 $\mu$m long. The trenches are then etched through the n+ ion implanted material **25**, the p-type channel layer **24**, and into the n- drain region **23** in 100% of nitrogen trifluoride ($NF_3$) per 10% of nitrous oxide ($N_2O$); the depth of the etch is about 3.0 $\mu$m. The Al is then stripped and a fresh layer of Al is deposited and patterned once again in the pattern of the outer mesa termination **35**. The material outside the mesa is etched about 7.2 $\mu$m deep, again using reactive ion etching ("RIE") with $NF_3$ penetrating all of the epilayers grown.

The wafers are then oxidized in wet oxygen ($O_2$) at 1100°C for 30 minutes to form the gate oxide **31** and outer sidewall passivation layers **35**. The oxide thickness on the top of the mesas is about 80 nanometers (nm) thick and, based on oxide breakdown calculations, the sidewall oxide thickness is about 40 nm thick. A 300 nm thick layer of a metal such as molybdenum (Mo) is then deposited on the wafers and is patterned to form the gate contact **30** by an appropriate technique, for example wet etching in a phosphoric/nitric/acetic acid mixture. The gate layer may also be formed of polysilicon. The 65 nm thick

nickel (Ni) source contacts **26** are then deposited by first reactive ion etching the silicon dioxide ($SiO_2$) layer **31** in fluoroform ($CHF_3$) through windows in a photoresist and then depositing and lifting-off the Ni. The oxide is then etched off of the backside of the wafer and a 200 nm thick film of Ni is deposited on it for the drain contact **32**.

The wafers are then annealed for two minutes in Ar per 4% of hydrogen ($H_2$) at 800°C. After annealing, oxidation resistant overlayers (not shown in the Figures) are then sputtered onto the wafers. The source **26** and gate contacts **30** are coated with Titanium (Ti)/Platinum (Pt)/Gold (Au) in an undersized pattern using the lift-off process. Likewise, the backs of the wafers are overcoated with Ti/Pt/Au.

Figures 2-4 illustrate grounded vertical MOSFETS **20'**, **20"**, **20'''** having a V-shaped gate contact ("VMOSFET") according to three other embodiments of the invention. These embodiments have similar elements as shown in Figure 1 and are designated prime ('), double prime ("), and triple prime (''') respectively. In the embodiment of Figure 2, the n+ source region **25'** is implanted in the p- channel region **24'**. The source contact **26'** is then formed on the n+ source **25'** and p-channel **26'** regions. In the embodiment of Figure 3, the n+ source region **25"** is epitaxially grown on the p-channel region **24"** as illustrated. A portion of the n+ source region **25"** is etched for contact with the p-channel region **24"**. The source contact **26"** is then formed on the n+ source region **25"** and the p- channel region **24"**. Also, in the embodiment of Figure 4, the n+ source region **25'''** is epitaxially grown on the p-channel region **24'''**. A p+ region **33** is then implanted into the n+ source region **25'''** for contact between the p- channel region **24'''** and the source contact **26'''**. It will also be apparent to those skilled in the art that the p+ implantated region **33** for contact between

the p- channel region 24''' and the source contact 26''' may also be used in the embodiments illustrated in Figures 1-3. Ion implantation techniques may be used, and particularly the high temperature ion implantation techniques shown in U.S. Patent 5,087,576 by Edmond et al. entitled "*Implantation And Electrical Activation Of Dopants Into Monocrystalline Silicon Carbide*" which is hereby incorporated by reference.

Figure 5 shows the I-V curve of one of the lowest resistance devices. Figure 5 is a plot of the drain current-voltage characteristics for the VMOSFET according to the present invention. Figure 6 is a plot of the transconductance-gate voltage characteristics of the same VMOSFET. This particular wafer had a channel doping of $p = 9.5 \times 10^{15}$ $cm^{-3}$ (9.5E15). An on-current of 40 milliamperes (mA) was achieved with a 2.3 voltage (V) drop when the gate voltage ($V_G$) was only +10 V, resulting in an on-resistance of 57 ohms ($\Omega$) (since the active area for the device is $6.7 \times 10^{-4}$ square centimeters ($cm^2$), the drain-to-source resistance ($R_{DS(on)}$) = 38 $m\Omega$-$cm^2$). The threshold voltage ($V_{th}$) of this device at room temperature ("RT") was 1.6 V and the maximum transconductance at drain voltage ($V_D$) = 18 V and $V_G$ = +10 V was 24 milliSiemens (mS) (6.0 mS/millimeter (mm)).

These devices were also characterized as a function of temperature. Another low doped power device had a RT $V_{th}$ of 3.2 V and transconductance of 5 mS/mm. The $R_{DS(on)}$ of this device at $V_G$ = +10 V was 49.6 $m\Omega$-$cm^2$. The $V_{th}$ dropped rapidly between RT and 150 degrees Centigrade (°C ) to 1.7 V and the $R_{DS(on)}$ decreased and then began to rise, with a value of 46.2 $m\Omega$-$cm^2$ at 150°C. The transconductance dropped to 3.5 mS/mm at this temperature. These devices operated well to 300°C. At this temperature, the voltage stabilized at about 1.6 V. The $R_{DS(on)}$ increased to 60 $m\Omega$-$cm^2$ and the transconductance decreased to 2.75 mS/mm. The

device characteristics returned to their original characteristics after they were cooled down.

Accordingly, various oxidation techniques may also be used for these devices such as shown in copending U.S. Patent Serial No. 07/893,642 entitled "*Method Of Obtaining High Quality Silicon Dioxide Passivation On Silicon Carbide And Resulting Passivated Structures*" filed on June 5, 1992 by the same inventor. This copending application is hereby incorporated herein by reference. These views illustrate V-shaped gate contacts for the MOSFET, but other various forms such as Double Diffused Metal Oxide Semiconductors (DDMOS) or planar MOSFETS may also be used. It has also been found that use of Al p-type oxidation causes low channel mobility in a thermally grown oxide because of high interface trap density at the $SiO_2$/SiC interface. Further, the doping levels for forming the illustrated embodiments may range from $2E^{15}$ to $5E^{18}$ atoms/$cm^3$.

Accordingly, vertical power MOSFETs were also fabricated with higher channel doping using the above referenced oxidation techniques as opposed to the low channel doping of the previous embodiments using conventional doping techniques. A thin layer of deposited polysilicon was used as the sacrificial layer prior to oxidation. In such use, polysilicon has several advantages over epitaxially grown undoped SiC. In addition to the more uniform coatings that are obtained, the resulting thermal oxides do not contain any of the various carbon oxide ($CO_x$) by-products of SiC oxidation. Also, the oxidation can be carried out at lower temperatures, but may also be for shorter times or both. Since Si oxidizes much faster than SiC, the polysilicon is consumed fairly rapidly, but the $SiO_2$ essentially stops when it reaches the SiC interface. Therefore, virtually no SiC is consumed, but the high quality of a thermal $SiO_2$/SiC interface will be

obtained. While the presence of Al at this interface is still likely to cause interface states, the problem can be minimized as much as possible.

The wafers were grown on Si-face n+ wafers with a dopant density of 2.5-3 x $10^{18}$ $cm^{-3}$ (2.5-3E18). The epitaxial structure of these wafers was similar to that previously described, except the drain region had a doping of n = 1-2 x $10^{16}$ $cm^{-3}$ (1-2E16) and the p-type channel doping ranged from 1-1.7 x $10^{17}$ $cm^{-3}$ (1-1.7E17) and was 1.0 $\mu$m thick.

The device fabrication for these wafers was also similar to that described for the structures discussed earlier with low channel doping. The only differences were in the implant and oxidation conditions. The implants were made shallower since the oxide growth would not remove any material. The resulting gate length was about 0.5 $\mu$m. These conditions were:

E = 25 keV, $\phi$ = 9.02 x 1014 cm-2

E = 40 keV, $\phi$ = 1.34 x 1015 cm-2

E = 80 keV, $\phi$ = 2.17 x 1015 cm-2

E = 150 keV, $\phi$ = 3.11 x 1015 cm-2.

Also, the trenches were only etched to a depth of 1.3 $\mu$m because of the thinner p- layer. After the formation of the trenches and the mesas, the 40 nm thick sacrificial polysilicon layer was deposited, via low-pressure chemical vapor deposition ("LPCVD"). This layer was then oxidized at 1100°C in wet $O_2$ for 9 minutes. The resulting oxide thickness was 78 nm thick. The rest of the device processing was identical to that described earlier.

The channel doping for one particular wafer was p = 1.2 x $10^{17}$ $cm^{-3}$ (1.2E17). An on-current of 22 mA was achieved at room temperature with a gate voltage of +16 V. The on-resistance at this gate voltage was 184 $\Omega$, giving an $R_{DS(on)}$ = 123 m$\Omega$-$cm^2$. The threshold voltage of this device at room temperature was 7.5 V and the

maximum transconductance at $V_D$ = 20 V and $V_G$ = +16 V was 6.8 mS (1.7 mS/mm). Although these numbers are not as good as those discussed earlier, it should be noted that the oxides are about twice as thick for these devices, which has a significant impact on decreasing the transconductance. The room temperature channel mobility estimated for this device was about 2.2 $cm^2$/V-seconds.

The low channel mobilities were found to arise with high levels of Al doping for the channel region due to the high interface trap density caused by the Al at the $SiO_2$/SiC interface. Although the inventors do not want to be bound by a particular theory, it appears that the use of boron (B) for doping of the channel region will reduce these low channel mobility problems. Hence, it will be apparent to those skilled in the art that B doping may be used herein where Al is described.

These devices were also characterized as a function of temperature. The decrease in threshold voltage for these devices was quite stable with increasing temperature. At 150°C, $V_{th}$ decreased to 6.7 V and the $R_{DS(on)}$ had slightly decreased to 117 mΩ-$cm^2$. The transconductance increased slightly to 1.8 mS/mm at this temperature. These devices also operated well to 300°C. At this temperature the $V_{th}$ had further decreased to about 6.3 V. The $R_{DS(on)}$ remained stable at 117 mΩ-$cm^2$ and the transconductance had increased to 2.0 mS/mm.

The $V_{th}$ is quite well behaved for both sets of devices, and are very close to the calculated values given the doping densities used. The average rate of decrease for the heavily doped device was about 4-5 millivolts (mV)/°C which is about the same rate observed for Si MOSFETs. While $V_{th}$ for the low doped samples dropped rapidly from room temperature to 100°C,

it then remained very stable with increasing temperature.

The transconductance for the high doped channel layers increased with temperature to about 200°C. This indicated that the devices were still dominated by the interface traps at RT and that they were being overcome at high temperature. The low doped samples showed very high RT transconductances that decreased with temperature. This is much closer to the ideal case, where the traps do not dominate the characteristics and transconductance drops with increasing temperature due to decreasing mobility.

Based on the best and most recent results obtained for the vertical MOSFETs with low channel doping ($R_{DS(on)}$ = 37.5 mΩ-cm$^2$), a 20 ampere (A) power MOSFET would have a die size of about 4 millimeters (mm) x 4 mm for a 5 V drop. It is expected that better performance will occur so that a 1000V power MOSFET with an $R_{DS(on)}$ of 0.9 mΩ-cm$^2$ may be provided.

Figure 7 is an ungrounded VMOSFET according to yet another embodiment of the present invention. Although this is not the optimal structure, it allows all of the doping to be done via epitaxy and negates the need for ion implantation. The fabrication procedures are identical to those described earlier, except the ion implantation is eliminated. The oxides were conventionally grown from the SiC in wet $O_2$.

The first vertical devices fabricated with this structure did operate, but showed high gate leakage currents and the threshold voltages exceeded +10 V. Excessive leakage current was observed at drain biases higher than 25 V. The measured specific on-resistance of these devices at $V_G$ = 22 V was approximately 350 mΩ-cm$^2$. The high threshold voltage observed for these devices was due to the relatively high channel doping of p = 1 x $10^{17}$ cm$^{-3}$ (1E17). It was assumed that this heavy channel doping contributed to

the low channel mobility by causing a high density of interface traps which, in turn, cause the low transconductance and high $R_{DS(on)}$, due to the degrading effects of Al in oxides as discussed earlier. The reason for doping the channel heavily was to allow short (submicron) gate lengths to be used with a 50-100 V bias, as is conventionally done for Si power MOSFETs. Based on the performance of these devices, the next set of wafers were grown with thicker (1.4 $\mu$m), lower doped channel regions with p = 1-2 x $10^{16}$ $cm^{-3}$ (1-2E16). The drain regions were doped at approximately n = 3-8 x $10^{15}$ $cm^{-3}$ (3-8E15) and were 5 $\mu$m thick. These thicknesses allowed 50 V operation before the depletion region punched through the drain to the n+ substrate.

These devices had much better characteristics than the heavily doped devices, but it was found that the lack of grounding on the channel layer influenced the I-V characteristics dramatically. The I-V curves showed very little current saturation until a drain voltage of about 60 V was reached. Very high resistance (13,000-15,000 Ω) was observed in the linear region of the curves. These characteristics improved dramatically when the devices were illuminated with a tungsten lamp. The linear region had a much lower resistance of 1150 Ω and the curves reach a saturation condition at less than $V_D$ = 10 V, although the saturation was rather sloped (output resistance = 15,000 Ω). It is suspected that the illumination creates some electron-hole pairs at the p-n junctions that allow some bleeding off of the channel charge, causing a grounding effect. Likewise, the higher drain voltages cause more junction leakage, which also effectively grounds the channel layer. Although these RT characteristics are generally undesirable, these devices are expected to operate well at higher temperatures because the higher junction leakage currents allow grounding of the channel layer.

Figure 8 shows a typical set of I-V curves obtained for one of these ungrounded devices under illumination. Figure 8 is a plot of the current-voltage characteristics for an ungrounded VMOSFET having a gate length of 1.4 $\mu$m and a gate periphery of 4 mm according to another embodiment of the present invention. This device had a channel doping of about p=1.3 x $10^{16}$ $cm^{-3}$ (1.3E16). The threshold voltage was $V_{th}$ = +5.5 V and the maximum transconductance was 1.57 mS (about 0.39 mS/mm). The resistance in the linear region was about 635 $\Omega$, which corresponds to an $R_{DS(on)}$ of about 430 m$\Omega$-$cm^2$ at $V_G$ = 19 V.

Figure 9 is a photographic view of the interdigitated mask design used to form a MOSFET according to the present invention. The mask design for these small area devices has the multiple fingered trench design discussed earlier. The left contact pad with eight fingers is the gate contact. There is a 5 $\mu$m x 250 $\mu$m wide trench etched in each finger, with the 10 $\mu$m wide gate contact overlapping it. Surrounding the gate fingers are nine source contact fingers that come from the contact pad on the right. The large outline surrounding these fingers is where the mesa edge termination is etched through the epilayers down to the substrate. This mesa edge termination confines the depletion region in the drain-drift layer and its area is 1.03 x $10^{-3}$ $cm^{-2}$. The active area of the device, however, where the source and gate fingers are located, is 6.7 x $10^{-4}$ $cm^{-2}$. Although the mask was used for the UMOS devices, the other VMOS cross-sectional designs, such as shown in Figures 2-4 and 7, may also use an interdigitated mask for forming the MOSFET. Further, it will be apparent to those skilled in the art that other various structures, such as square or hexagonal cells, may also be used for forming various MOSFET structures according to the present invention.

In the drawings and specification, there has been disclosed a typical preferred embodiment of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for the purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. A power metal oxide semiconductor field effect transistor (MOSFET) having a low on-resistance and a high temperature range, comprising:

a drain region of silicon carbide, said drain region having a substrate of silicon carbide and a drain-drift region of silicon carbide adjacent said substrate;

a channel region of silicon carbide adjacent said drain-drift region and having the opposite conductivity type from said drain-drift region;

a source region of silicon carbide adjacent said channel region and having a same conductivity type as said drain-drift region;

an insulating layer adjacent said channel region;

a gate region formed adjacent said insulating layer;

a source electrode formed adjacent a second portion of said source region; and

a drain electrode formed adjacent a second portion of said drain region.

2. A MOSFET according to Claim 1, wherein said source electrode extends adjacent a second portion of said channel region.

3. A MOSFET according to Claim 1 or 2, wherein said substrate of said drain region is formed of silicon carbide having a first conductivity type and said drain-drift region of said drain region is formed of silicon carbide having said first conductivity type.

4. A MOSFET according to Claim 1 or 2, wherein said substrate of said drain region is formed of silicon carbide having a first conductivity type and said drain-drift region of said drain region is formed

of silicon carbide having the opposite conductivity type.

5. A MOSFET according to Claim 1 or 2, further comprising a mesa edge termination of said source, said channel, and said drain-drift regions.

6. A MOSFET according to Claim 1, wherein said insulating layer comprises silicon dioxide.

7. A MOSFET according to Claim 1, wherein at least one of said regions of silicon carbide has a polytype selected from the group consisting of 3C, 2H, 4H, 6H, and 15R.

8. A MOSFET according to Claim 1, 2, 3, or 4, wherein said first conductivity type comprises n-type silicon carbide and said opposite conductivity type comprises p-type silicon carbide.

9. A MOSFET according to Claim 1, 2, 3, or 4, wherein said first conductivity type comprises p-type silicon carbide and said opposite conductivity type comprises n-type silicon carbide.

10. A MOSFET according to Claim 1, wherein said source and drain electrodes comprise nickel.

11. A MOSFET according to Claim 1, wherein said gate electrode comprises a gate contact formed of metal.

12. A MOSFET according to Claim 1, wherein said gate electrode comprises a gate contact formed of polysilicon.

13. A MOSFET according to Claim 1 or 2, wherein said channel layer is doped with aluminum.

14. A MOSFET according to Claim 1 or 2, wherein said channel layer is doped with boron.

15. A MOSFET according to Claim 1 or 2, wherein said channel region has a doping range from 2E15 to 5E18 atoms/$cm^3$.

16. A vertical power metal oxide semiconductor field effect transistor (MOSFET) having a low on-resistance and a high temperature range, comprising:

a substrate of silicon carbide having a first conductivity type;

a first layer of silicon carbide on said substrate and having said first conductivity type for forming a drain-drift region;

a second layer of silicon carbide on said first layer and having a second conductivity type, said second layer forming a channel region;

a third layer of silicon carbide on said second layer and having said first conductivity type, said third layer forming a source region;

an insulating layer on first portions of said drain, said channel, and said source regions;

a gate electrode on said insulating layer.

a source electrode formed on a second portion of said source region; and

a drain electrode formed on a second portion of said drain region.

17. A vertical power MOSFET according to Claim 16, wherein said source electrode extends on a second portion of said channel region.

18. A vertical power MOSFET according to Claim 16, further comprising a mesa edge termination of said source, said channel, and said drain-drift regions.

19. A vertical power MOSFET according to Claim 16, wherein at least one of said regions of silicon carbide has a polytype selected from the group consisting of 3C, 2H, 4H, 6H, and 15R.

20. A vertical power MOSFET according to Claim 16, wherein said first conductivity type comprises n-type silicon carbide and said opposite conductivity type comprises p-type silicon carbide.

21. A vertical power MOSFET according to Claim 16, wherein said first conductivity type comprises p-type silicon carbide and said opposite conductivity type comprises n-type silicon carbide.

22. A vertical power MOSFET according to Claim 16, wherein said channel region is doped with aluminum.

23. A vertical power MOSFET according to Claim 16, wherein said channel region is doped with boron.

24. A vertical power MOSFET according to Claim 16, wherein said channel region has a doping range from 2E15 to 5E18 atoms/$cm^3$.

25. A vertical power metal oxide semiconductor field effect transistor (MOSFET) having a low on-resistance and a high temperature range, comprising:

a drain region formed of silicon carbide, said drain region having a substrate of silicon carbide of a first conductivity type and a drain-drift region of silicon carbide on said substrate having said first conductivity type;

a channel region on said drain-drift region formed of silicon carbide and having a second conductivity type from said drain-drift region;

a source region on said channel region and having said first conductivity type;

a source electrode formed on a first portion of said source region;

a drain electrode formed on a first portion of said drain region;

a trench formed in second portions of said drain and source regions and in said first portion of said drain region; and

a gate region formed on said trench and adjacent second portions of said drain and source regions and in said first portion of said channel region.

26. A vertical power MOSFET according to Claim 25, wherein said source electrode extends on a second portion of said channel region.

27. A vertical power MOSFET according to Claim 25, further comprising a mesa edge termination of said source, said channel, and said drain-drift regions.

28. A vertical power MOSFET according to Claim 25, wherein said first conductivity type comprises n-type silicon carbide and said second conductivity type comprises p-type silicon carbide.

29. A vertical power MOSFET according to Claim 25, wherein said first conductivity type comprises p-type silicon carbide and said second conductivity type comprises n-type silicon carbide.

30. A vertical power MOSFET according to Claim 25, wherein said channel region is doped with aluminum.

31. A vertical power MOSFET according to Claim 25, wherein said channel region is doped with boron.

32. A vertical power MOSFET according to Claim 25, wherein said channel region has a doping range from 2E15 to 5E18 atoms/$cm^3$.

33. A vertical power MOSFET according to Claim 25, wherein said trench has a substantially U-shape.

34. A vertical power MOSFET according to Claim 25, wherein said trench has a substantially V-shape.

35. A method of fabricating a power metal oxide semiconductor field effect transistor (MOSFET) having a low on-resistance and a high temperature range, comprising the steps of:

forming a first region of silicon carbide having a first conductivity type for defining a drain region;

forming a second region of silicon carbide adjacent said first region having a second conductivity type for defining a channel region;

forming a third region of silicon carbide adjacent said second region, said third region having said first conductivity type for forming a source region;

forming an insulating layer adjacent said channel region; and

forming a gate layer adjacent said insulating layer.

36. A method according to Claim 35, further comprising the step of forming a mesa edge termination of said source, said channel, and said drain-drift regions.

37. A method according to Claim 35, wherein at least one of said regions of silicon carbide has a polytype selected from the group consisting of 3C, 2H, 4H, 6H, and 15R.

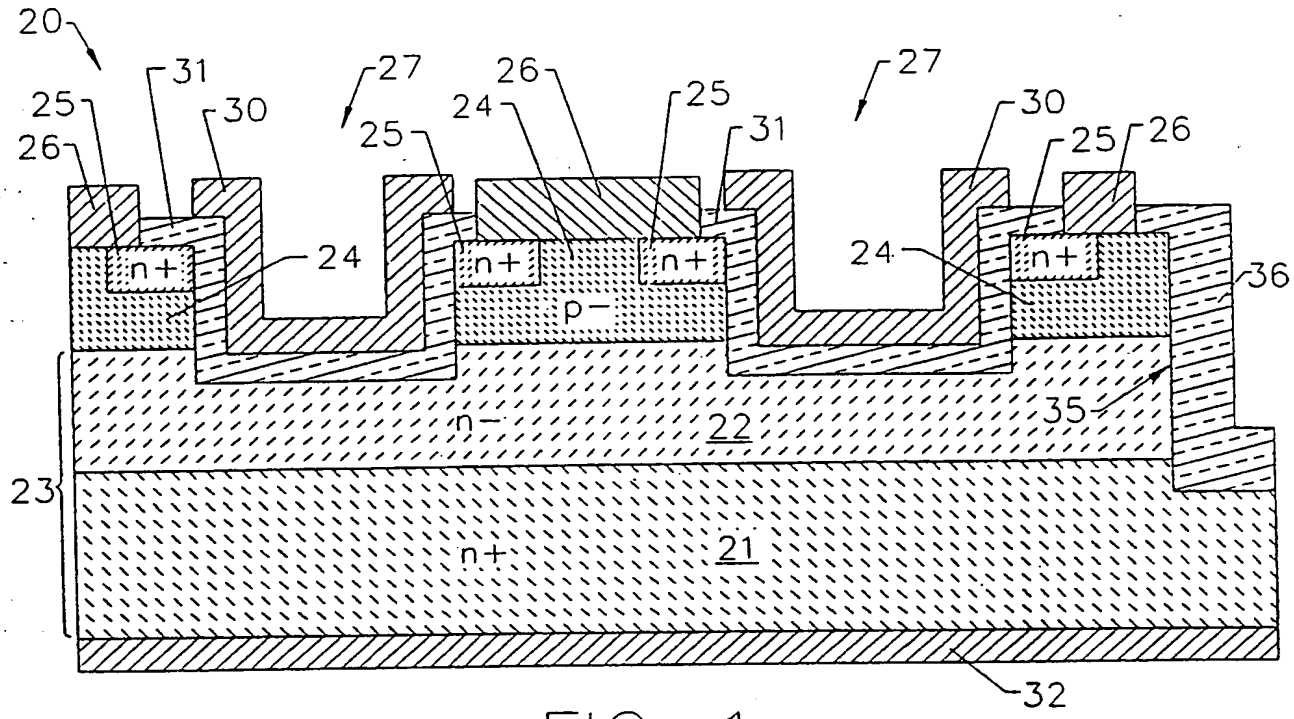
38. A method according to Claim 35, wherein the step of forming the region of silicon carbide comprises the step of epitaxially growing the silicon carbide on the previous layer.

39. A method according to Claim 35, wherein the step of forming a third region of silicon carbide comprises the step of implanting silicon carbide at a high temperature in a portion of the second region of silicon carbide.

40. A method according to Claim 35, further comprising the steps of:

forming a source contact to the source region; and

forming a drain contact to the drain region.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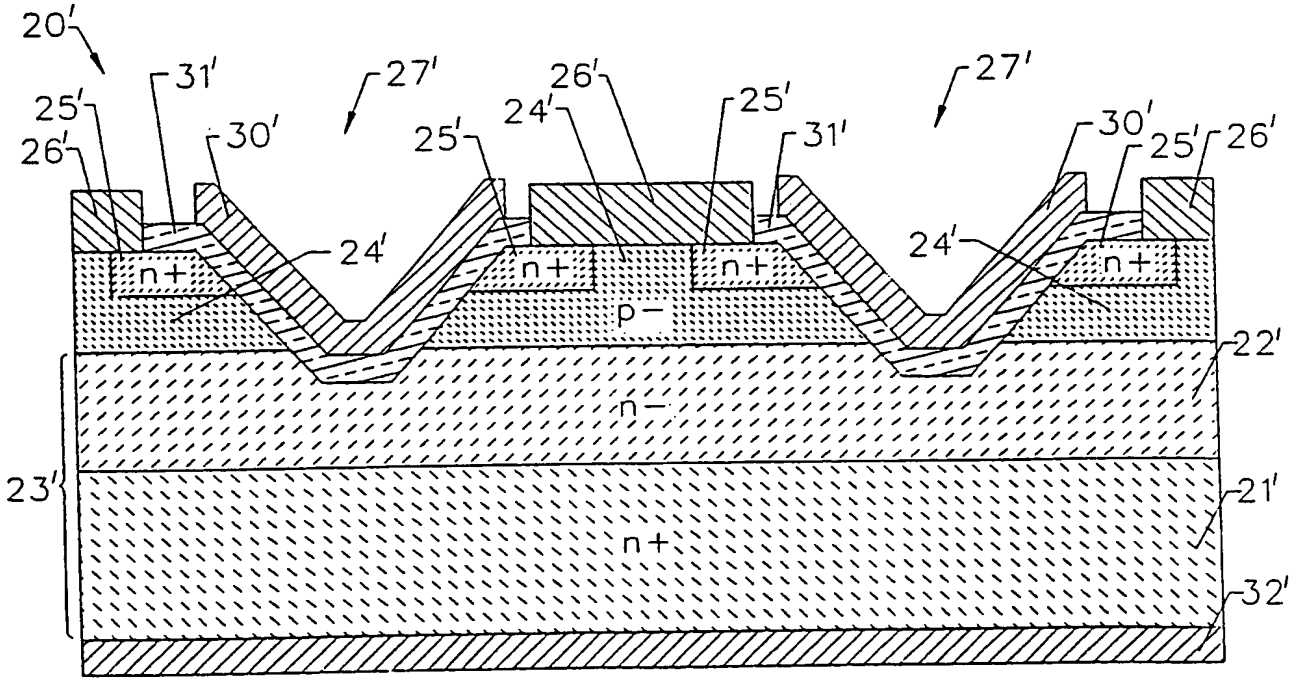
31
27
26
25
30
24
25
25
26
24
25
31
27
30
25
26
n+
n+
n+
n+
24
36
p−
n−
22
35
23
n+
21
32

FIG. 1.


20'
31'
27'
26'
25'
30'
24'
25'
25'
26'
24'
25'
31'
27'
30'
25'
26'
n+
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n+
n+
24'
22'
p−
n−
23'
21'
n+
32'

FIG. 2.

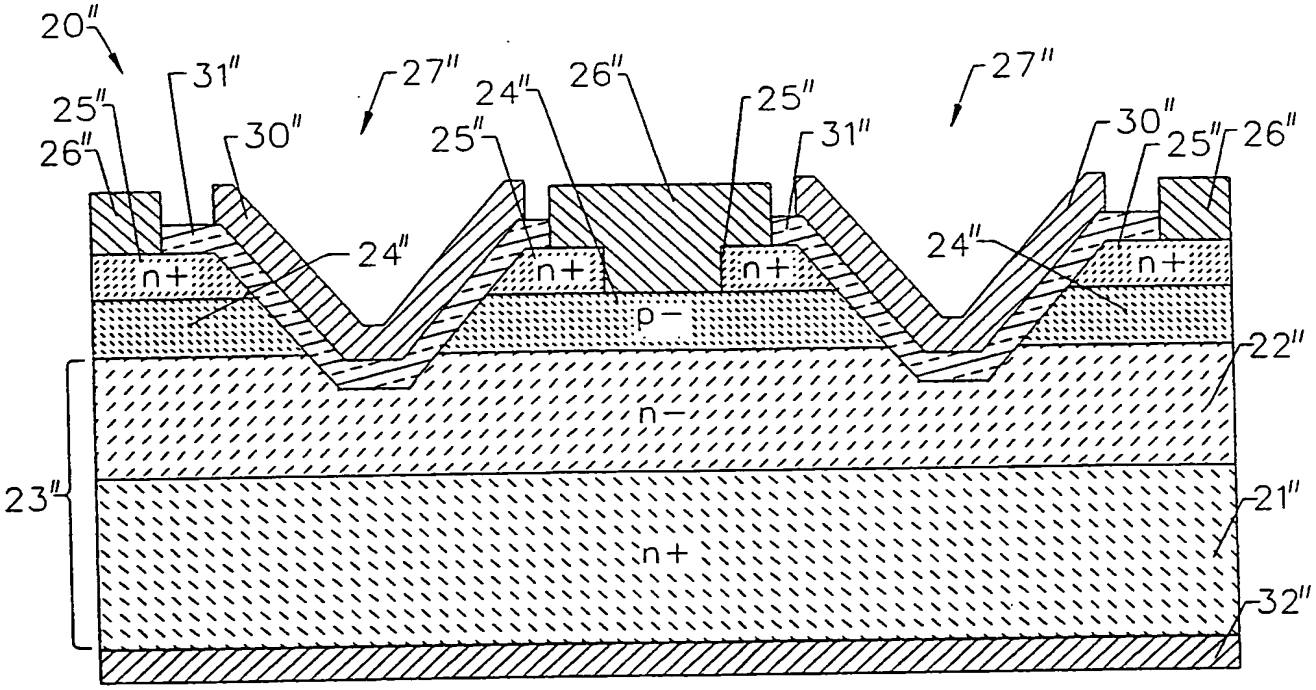
20"
31"
27"
24"
26"
25"
30"
n+
p−
n−
22"
23"
21"
32"

FIG. 3.

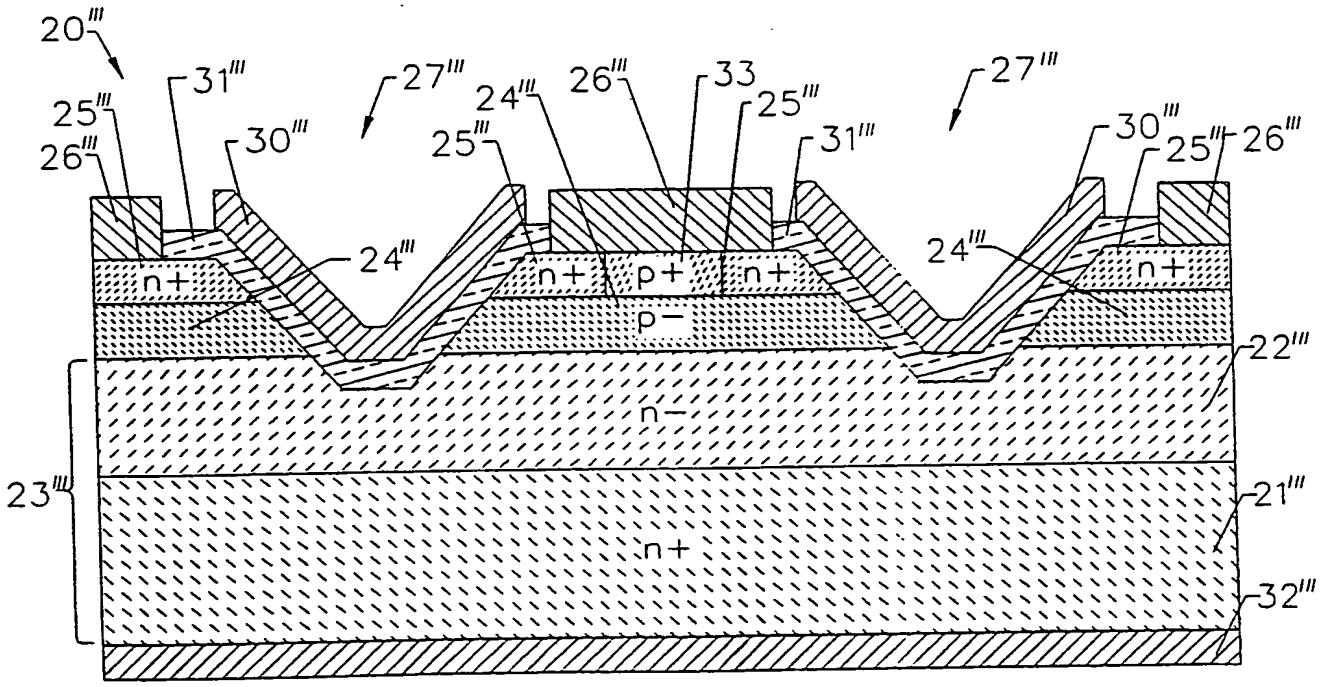
20'''
31'''
27'''
24'''
26'''
33
25'''
30'''
n+
p+
p−
n−
22'''
23'''
21'''
32'''

FIG. 4.

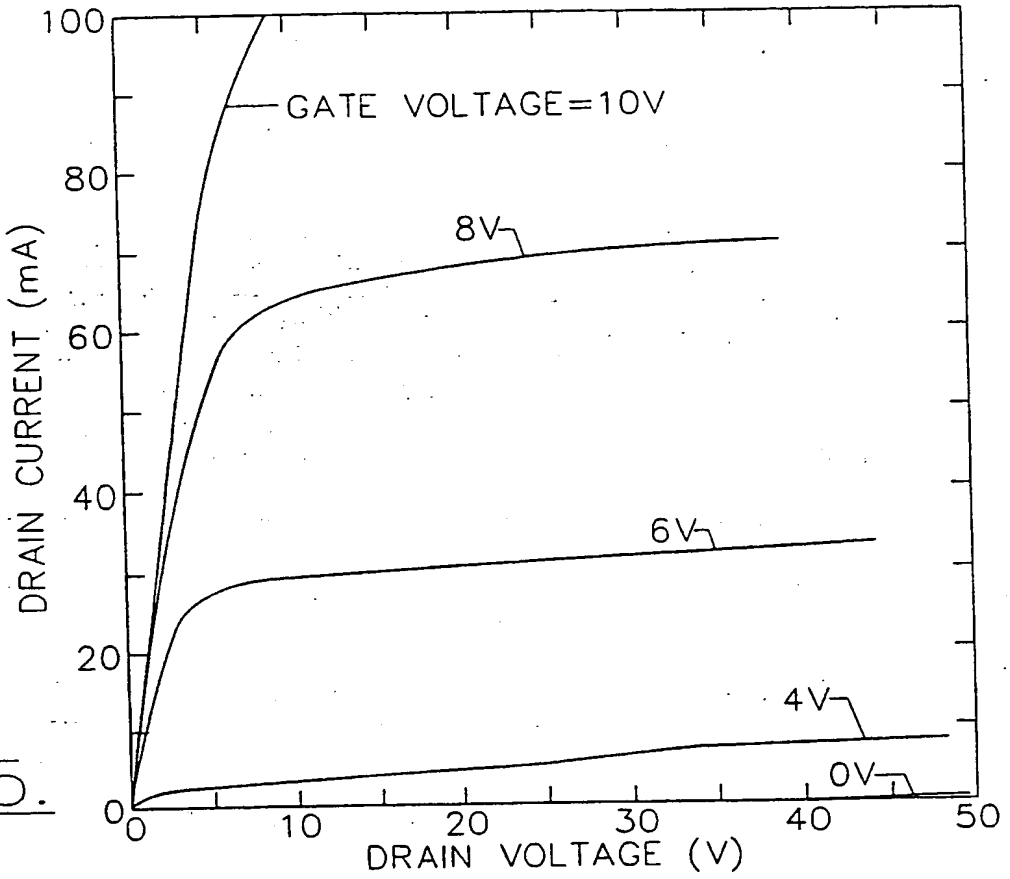
100
80
60
40
20
0
0
10
20
30
40
50
DRAIN CURRENT (mA)
DRAIN VOLTAGE (V)
GATE VOLTAGE=10V
8V
6V
4V
0V

FIG. 5.

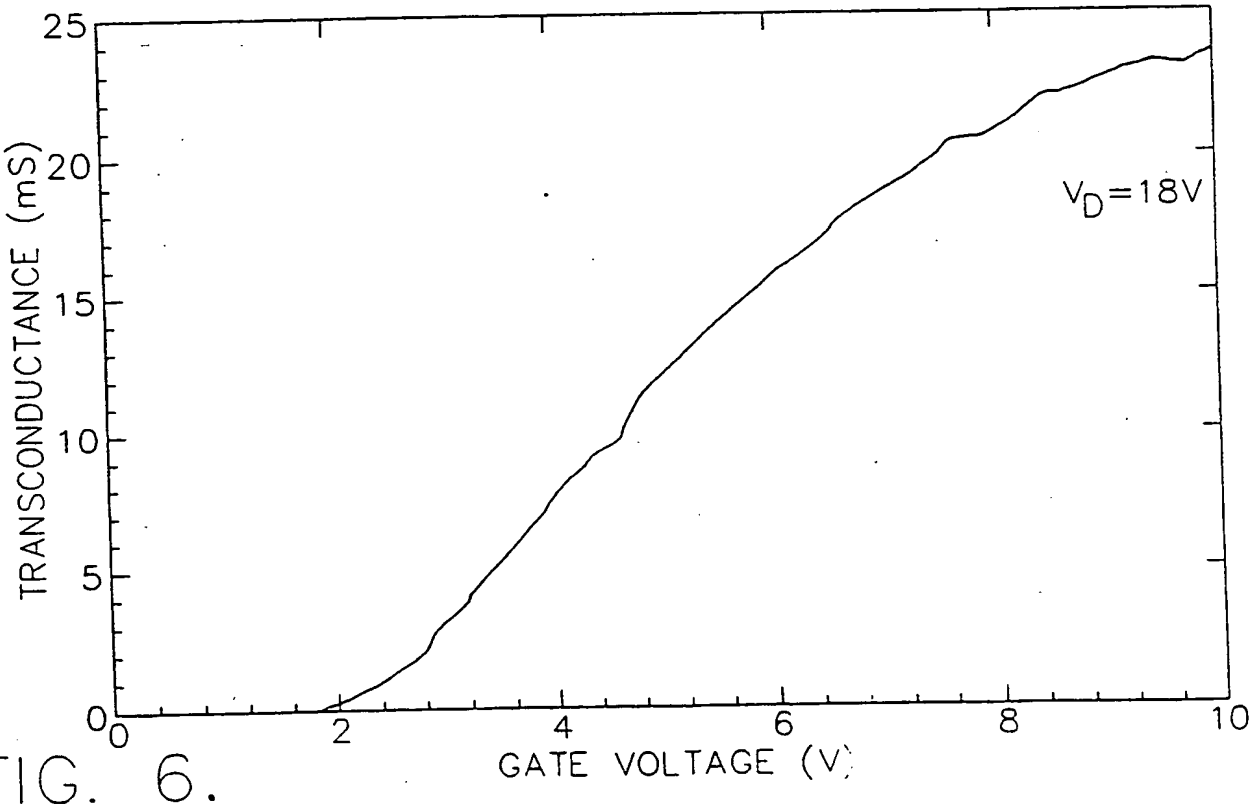
25
20
15
10
5
0
0
2
4
6
8
10
TRANSCONDUCTANCE (mS)
GATE VOLTAGE (V)
$V_D$=18V

FIG. 6.

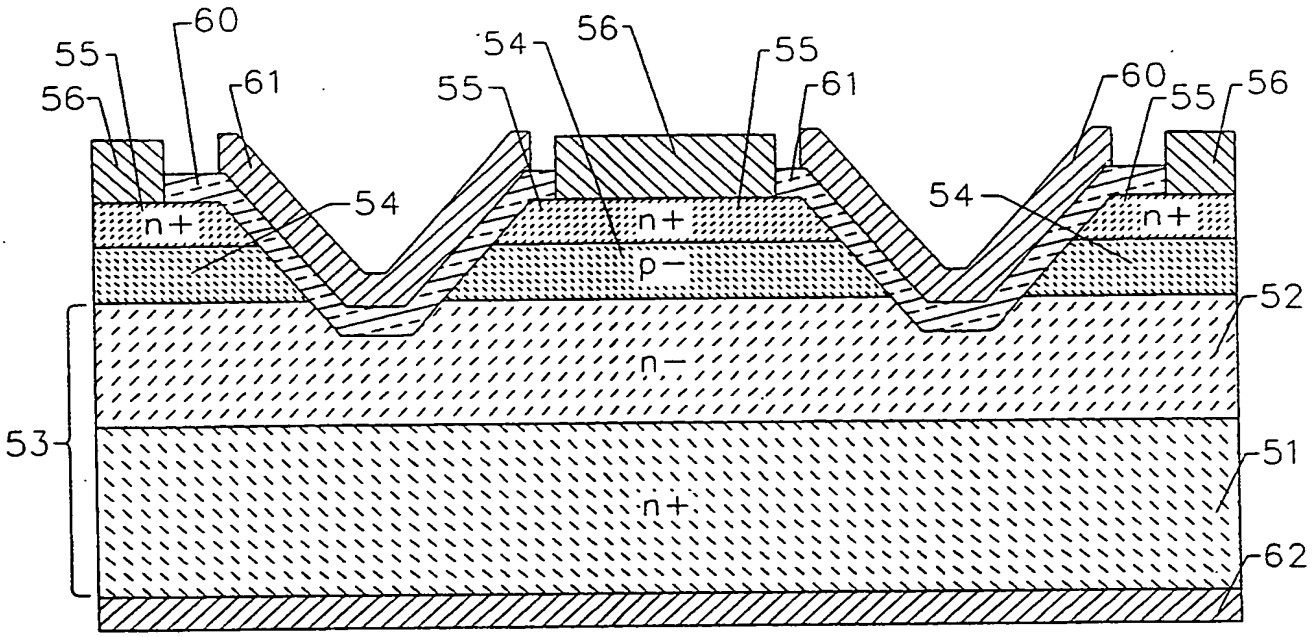
60
55
56
61
54
56
55
55
61
60
55
56
54
54
n+
n+
n+
p−
52
n−
53
51
n+
62

FIG. 7.

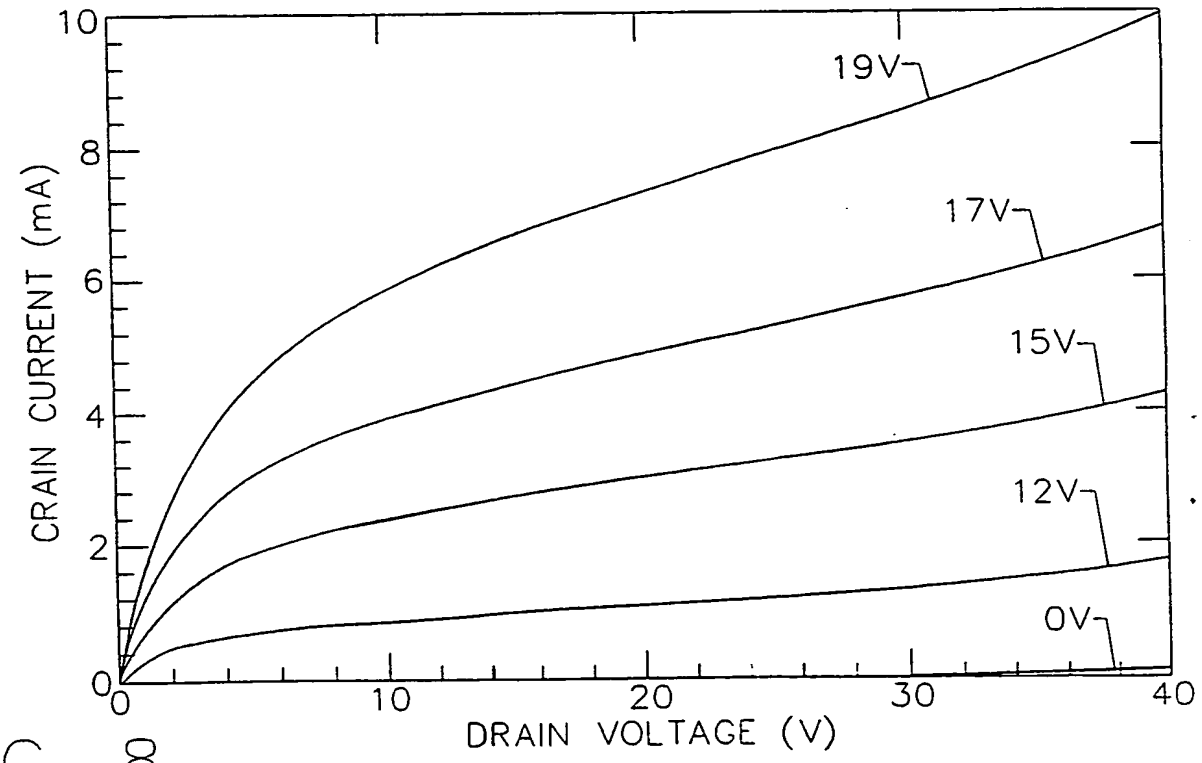
10
8
6
4
2
0
CRAIN CURRENT (mA)
19V
17V
15V
12V
0V
0
10
20
30
40
DRAIN VOLTAGE (V)

FIG. 8.

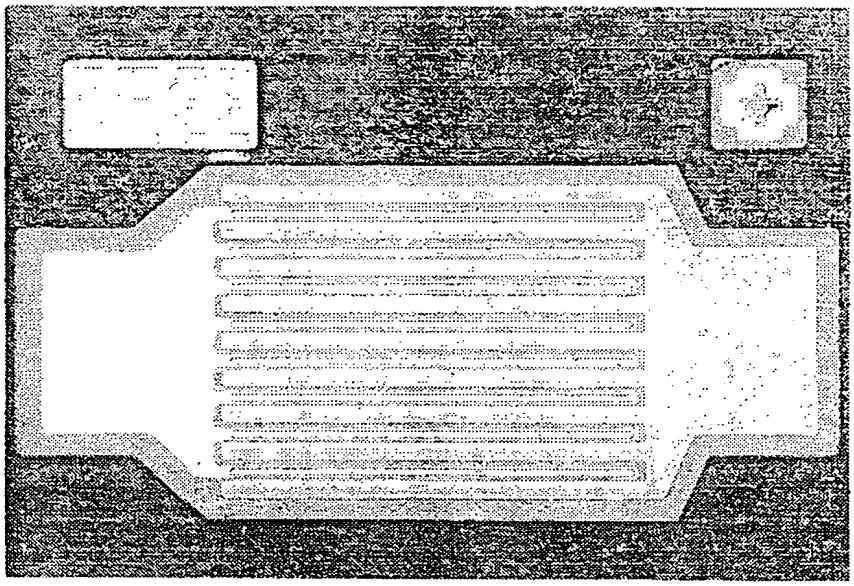

FIG. 9.

# INTERNATIONAL SEARCH REPORT

Intl. Application No
PCT/US 93/10490

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H01L29/24 H01L29/784

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN<br>vol. 017, no. 006 (E-1302)7 January 1993<br>& JP,A,04 239 778 (FUJI ELECTRIC CO LTD)<br>27 August 1992<br><br>see abstract<br>---<br>-/-- | 1-3,9,<br>16,17,<br>20,21,<br>25,26,<br>28,29,<br>33,35,<br>39,40 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 31 January 1994 | 07.02.94 |

| Name and mailing address of the ISA | Authorized officer |
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| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax (+ 31-70) 340-3016 | Mimoun, B |

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN<br>vol. 016, no. 196 (E-1200)12 May 1992<br>& JP,A,04 029 368 (SHARP CORP) 31 January 1992<br><br>see abstract<br>& US,A,5 170 231 (FUJII ET AL) 8 December 1992 | 1,3,7,9,<br>10,12,<br>13,15,<br>16,19,<br>20,22,<br>24,25,<br>28,30,<br>32,33,<br>35,37,<br>39,40 |
| E | WO,A,93 26047 (NORTH CAROLINA STATE UNIVERSITY) 23 December 1993<br><br>see the whole document<br>& US,A,5 233 215 (BALIGA) 3 August 1993 | 1,3,5,6,<br>9,12,16,<br>18-20,<br>25,27,<br>28,33,<br>35,36,<br>38,40 |
| A | JAPANESE JOURNAL OF APPLIED PHYSICS/PART 2: LETTERS<br>vol. 27, no. 11 , November 1988 , TOKYO JP<br>pages 21243 - 2145<br>HIROO FUMA ET AL 'High Temperature Operated Enhancement-Type beta-SiC MOSFET'<br>see the whole document | 1,6,11,<br>14,23,31 |
| A | EP,A,0 159 663 (GENERAL ELECTRIC COMPANY) 30 October 1985<br>see abstract; figure 1 | 1,34 |
| A | JOURNAL OF THE ELECTROCHEMICAL SOCIETY<br>vol. 137, no. 1 , January 1990 ,<br>MANCHESTER, NEW HAMPSHIRE US<br>pages 212 - 220<br>W.-S. PAN ET AL 'Reactive Ion Etching of SiC Thin Film by Mixtures of fluorinated Gases and Oxygen'<br>see page 216, column 2, paragraph 2 | 34 |

# INTERNATIONAL SEARCH REPORT

information on patent family members

Inte onal Application No
PCT/US 93/10490

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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| WO-A-9326047 | 23-12-93 | US-A- 5233215 | 03-08-93 |
| US-A-5233215 | 03-08-93 | WO-A- 9326047 | 23-12-93 |
| EP-A-0159663 | 30-10-85 | JP-A- 60253275 | 13-12-85 |